Digital Gate ICs for Driving and Sensing Power Devices to Achieve Low-Loss, Low-Noise, and Highly Reliable Power Electronic Systems

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Abstract—In order to shift the business of power electronics systems such as power converters using power devices from a sell-out type to a subscription type that provides the best service for each user, digital gate ICs that drive and sense power devices and are connected to the network will be a key technology. This paper presents several examples of the development of digital gate ICs that integrate a sensor, a controller, and a digital gate driver to digitally control gate current in fine time steps on a single chip.

1 Introduction

Fig. 1 shows a block diagram of a conventional power converter including a gate driver IC. The gate driver IC is a circuit that switches power devices by interfacing between a low-voltage controller and a high-voltage main circuit. Specifically, the gate driver IC drives the gate terminals of power devices by amplifying the 5-V amplitude on/off signal from the PWM controller IC to the gate voltage (V_{GE}) of 5 V to 18 V and the gate current (I_G) of 1 A to 20 A. Many gate driver ICs in products detect the over-current and/or over-voltage of IGBTs and output an alarm signal. Conventional gate driver ICs are too simple in functionality to enable a shift in the business of power electronics systems, such as power converters using power devices, from a sell-off of products to a subscription-based business that provides the best service for each user.

In contrast, Fig. 2 shows the proposed subscription-based service platform, where the key technology is a digital gate IC that drives and senses power devices and connected to a network. A sensor circuit integrated in a digital gate IC measures the operating conditions (e.g., I_C, V_{CE}, and junction temperature) and degradation status (e.g., threshold voltage and bond wire lift-off) of power devices and sends the measured results to the service provider's cloud over the network.

Service providers use AI to analyze sensor data from many users and provide the best service (e.g., digital gate driver parameters) for each user. This paper presents digital gate drivers developed to realize digital gate ICs, including a digital gate driver IC integrating dI_C/dt sensor and automatic timing control for IGBTs, a single-input dual-output digital gate driver IC for equalizing drain current of two parallel-connected SiC MOSFETs, and a large current output digital gate driver using half-bridge DAC IC and two power MOSFETs for IGBTs.

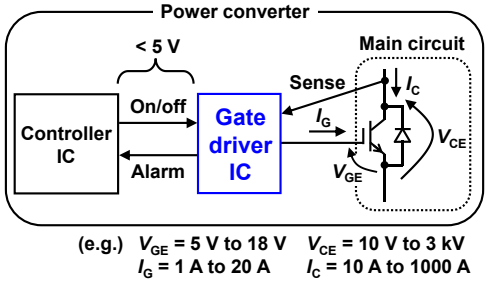

Fig. 1. Block diagram of conventional power converter including gate driver IC.

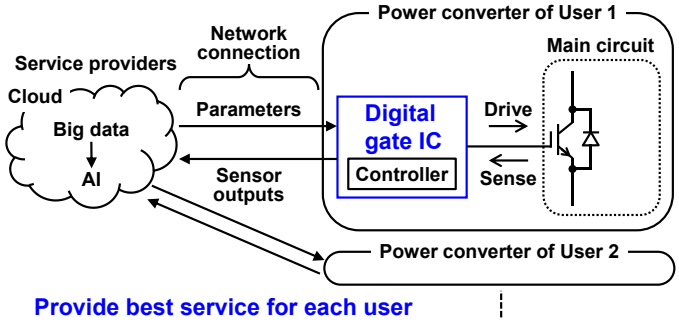

Fig. 2. Proposed subscription-based service platform, where key technology is digital gate IC.

2 Digital Gate Driver IC Integrating dI_C/dt Sensor and Automatic Timing Control for IGBTs

2-1 Research Motivation

A lot of active gate drivers (AGDs), where the gate driving waveform is controlled during the turn-on/off transients, have been proposed to reduce both the switching loss and the switching noise of power devices. AGDs can be classified into two types, open-loop control [1-6] and closed-loop control [7-19]. The closed-loop AGDs are required instead of the open-loop AGDs, because the optimal driving waveform changes depending on the operating conditions (e.g. load current and temperature) [20]. Fig. 3 summarizes the design choices in conventional closed-loop AGDs. To make the closed-loop AGDs practical, the following three points are required: (1) single-chip integration instead of PCB implementation for lower cost, (2) real-time control instead of iterative control to reliably handle dynamic change of operating conditions, and (3) programmable AGDs instead of fixed-function AGDs that require individual optimization for different product variety of power devices. In the closed-loop AGDs, however, no previous paper has realized (1) and (2) simultaneously, and no previous paper on (3) has been published.

To solve the problems, a digital gate driver (DGD) IC with fully integrated automatic timing control (ATC) function for IGBTs that realizes all of (1) to (3) is proposed [21]. The design choices in this work are shown in blue in Fig. 3.

2-2 Circuit Design

Figs. 4 and 5 show a circuit schematic and a timing chart of the proposed DGD IC with ATC, respectively. In the following, turn-on is discussed, whereas the exact same is true for turn-off. The IC includes dI_C/dt detector for the state change, controller for ATC, and a 6-bit current-source type digital gate driver with variable gate current (I_G) in 64 levels, where $I_G = n_{PMOS} \times 48$ mA and n_{PMOS} is an integer from 0 to 63. At turn-on, an active gate driving is performed

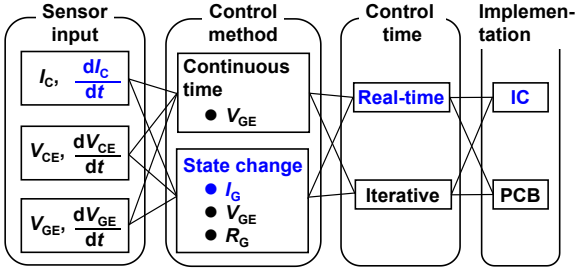

Fig. 3. Design choices in closed-loop AGDs. This work is shown in blue.

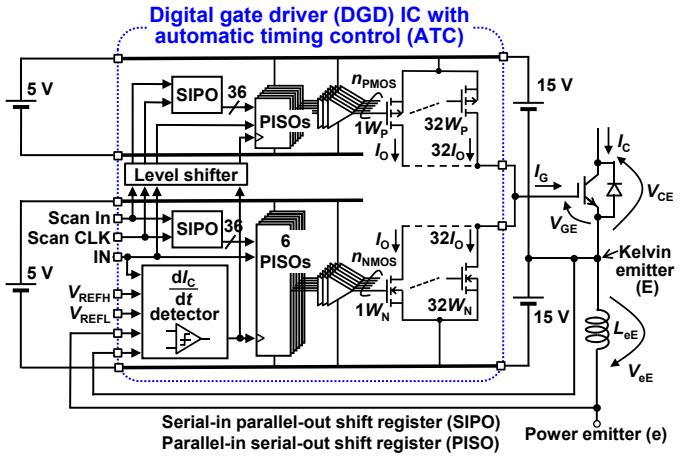

Fig. 4. Circuit schematic of proposed DGD IC with ATC.

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in three slots from t_1 to t_3 with different I_G of strong (n_1) -weak (n_2) -strong (n_3), and this driving method is defined as stop-and-go gate drive (SGGD) [22]. n_1 to n_3 are preset by a digital input (Scan In), while t_1 and t_2 are automatically determined by ATC. An important feature of this IC is the full integration of t_1 and t_2 real-time automatic control functions on a single chip. The real-time control of t_1 and t_2 is done by detecting dI_C/dt by sensing the voltage (V_{eE}) of the parasitic inductance (L_{eE}) between Kelvin emitter and power emitter in Fig. 4, because $V_{eE} = -L_{eE}(dI_C/dt)$, where I_C is the collector current. Specifically, as shown in Fig. 5, the end timing of t_1 is determined by detecting the negative V_{eE} at the beginning of I_C flow using a comparator with the reference voltage of V_{REFL}, and the end timing of t_2 is determined by detecting the positive V_{eE} at the timing immediately after I_C overshoots using a comparator with the reference voltage of V_{REFH}. Fig. 6 shows a die photo of DGD IC fabricated with 180-nm BCD process.

2-3 Measured Results

Figs. 7 and 8 show a circuit schematic and a measurement setup of the double pulse test using the developed DGD IC and an IGBT module (FS100R12N2T4, 1200 V, 100 A), respectively. Figs. 9 (a) and (b) show timing charts of the conventional single-step gate drive (SSGD) and the proposed SGGD for comparison, respectively. In SSGD, n_1 is varied, which emulates a conventional gate driver with varied gate resistance. In SGGD, (n_1, n_2, n_3) are preset to (27, 2, 27), and t_1 and t_2 are automatically determined by ATC. Figs. 10 (a) and (b) show the measured I_C and gate-emitter voltage (V_{GE}) waveforms in SGGD with ATC with varied load current (I_L) from 10 A to 80 A, respectively. Fig. 10 (c) shows the measured t_2 vs. I_L. It is clearly observed that as I_L increases, t_1 remains constant, while t_2 is automatically increased by ATC. Figs. 11 (a) to (c) show the measured switching loss (E_{LOSS}) vs. the collector current overshoot ($I_{OVERSHOOT}$) of the conventional SSGD and the proposed SGGD at I_L = 20 A, 50 A, and 80 A, respectively. The black curves show the trade-off curves of the conventional SSGD with varied n_1 from 2 to 63. In all cases, the proposed SGGD has lower E_{LOSS} and lower $I_{OVERSHOOT}$ than the conventional SSGD. In Fig. 11 (c), Point A to Point C are defined, where Point B is the proposed SGGD, and Point A and Point C are the conventional SSGD with n_1 = 4 and 63, respectively. $I_{OVERSHOOT}$ of Point A and Point B are almost the same. At I_L = 80 A, compared with the conventional SSGD, the proposed SGGD reduces E_{LOSS} by 38 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 18 % under E_{LOSS}-aligned condition. Figs. 12 (a) to (c) show the measured waveforms in Point A, Point B, and Point C in Fig. 11 (c), respectively. Fig. 12 (b) clearly shows that the start of I_C flow and I_C overshoot are properly detected by V_{eE}, and that SGGD is realized with t_1 and t_2 correctly controlled. Table I shows a comparison table of the closed-loop AGDs. This work is the first work achieving the fully integrated IC, the real-time control, and the programmable I_G in the closed-loop AGDs.

Table I Comparison table of closed-loop AGDs

	TPEL'15 [11]	TPEL'18 [12]	TPEL'21 [14]	ISSCC'19 [13]	ISSCC'21 [18]	This work [21]
Target power device	IGBT	IGBT	SiC MOSFET	Si MOSFET	GaN FET	IGBT
Sensor input	dI_C/dt, V_{CE}	dI_C/dt, V_{CE}	dI_C/dt	V_{DS}	V_{DD} of high-side gate driver	dI_C/dt
Feedback control target	V_{GE} waveform	Timing of state change	Timing of state change	Timing of state change	Timing of state change	Timing of state change
Real-time control	Yes	Yes	Yes	No	No	Yes
Number of states per switching		4	3	3	3	3
Preset parameters for each state		I_G	V_{GS}	R_G	I_G	I_G
Levels of parameter		NA	2	2	3	6 bit
Implementation	PCB	PCB	PCB	IC (Not fully integrated)*	IC (Fully integrated)	IC (Fully integrated)
IC Process				130 nm HV CMOS	500 nm, 600 V SOI**	180 nm BCD

*Voltage divider for V_{DS} is not integrated.
**High-voltage IC process with the same breakdown voltage as V_{CC} of main circuit is required.

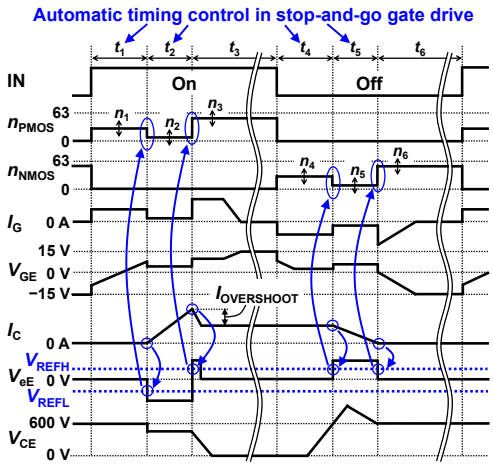


Fig. 5. Timing chart of proposed DGD IC with ATC.

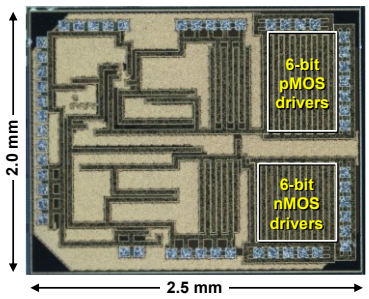


Fig. 6. Die photo of DGD IC with ATC.

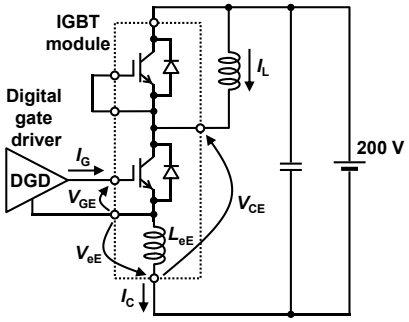


Fig. 7. Circuit schematic of double pulse test.

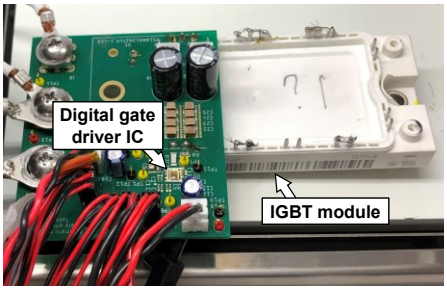
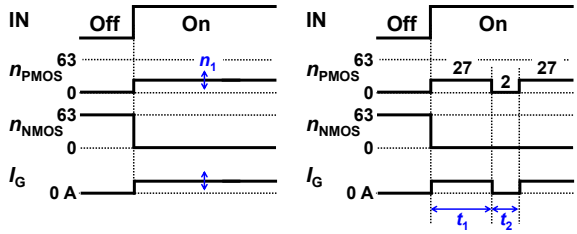


Fig. 8. Measurement setup.



(a) Conventional single-step gate drive (SSGD)

(b) Proposed stop-and-go gate drive (SGGD) with automatic timing control

Fig. 9. Timing charts for turn-on.

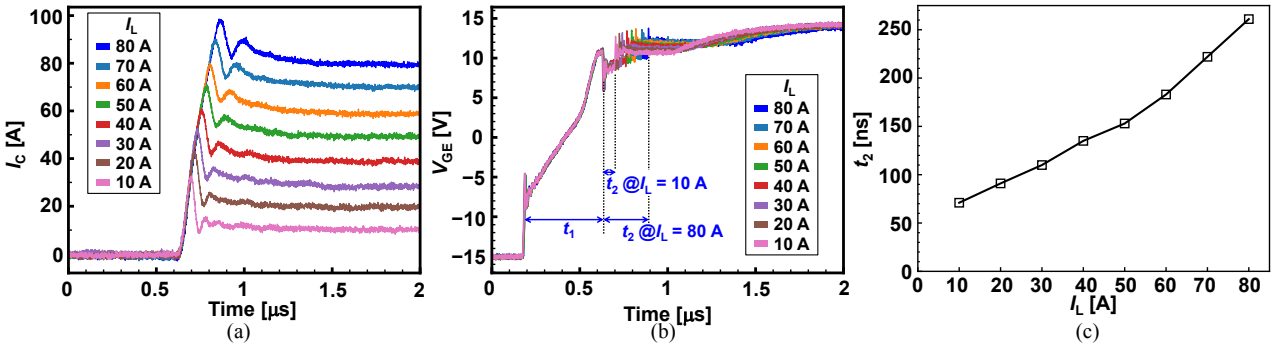


Fig. 10. Measured results in SGGD with ATC with varied I_L. (a) I_C waveforms. (b) V_{GE} waveforms. (c) t_2 vs. I_L.

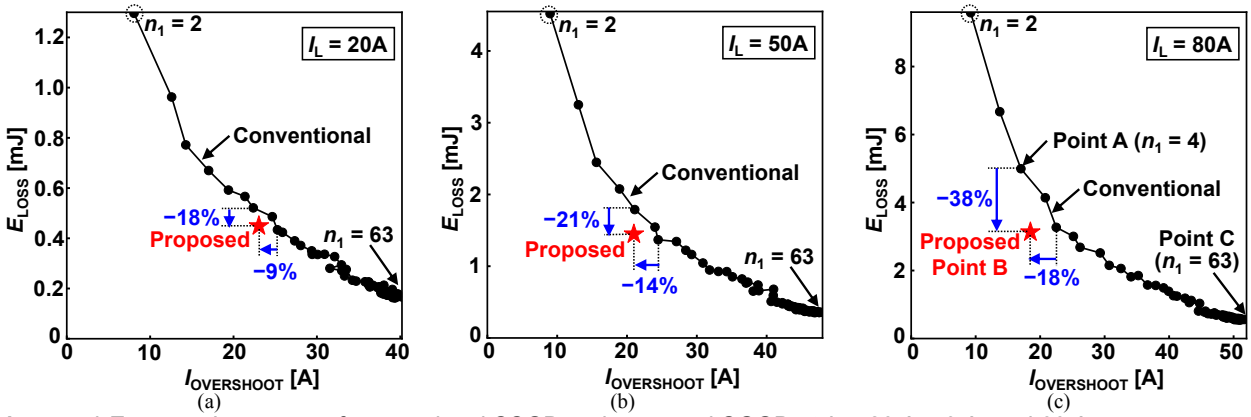


Fig. 11. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SSGD and proposed SGGD at I_L = 20 A, 50 A, and 80 A.

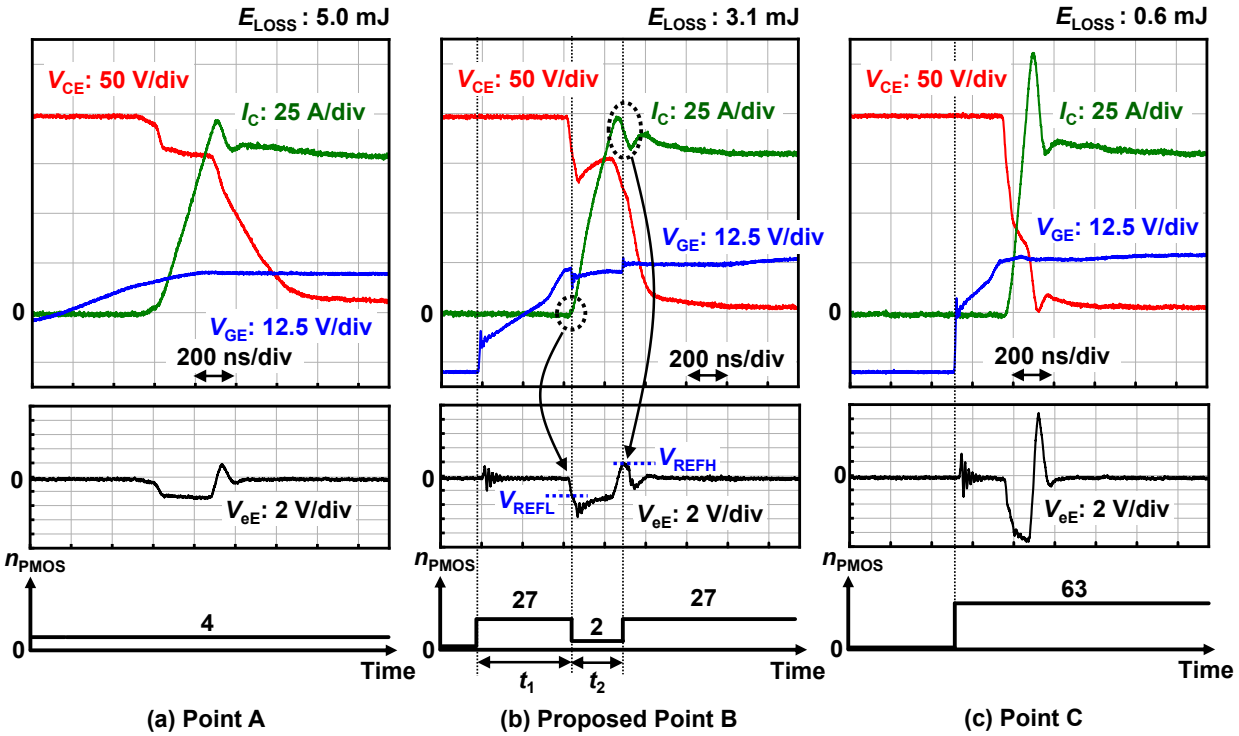


Fig. 12. Measured waveforms in Point A, Proposed Point B, and Point C in Fig. 11 (c) at I_L = 80 A.

3 Single-Input Dual-Output Digital Gate Driver IC for Equalizing Drain Current of Two Parallel-Connected SiC MOSFETs

3-1 Research Motivation

In power electronics systems, when large current exceeding the rated current of a power device is applied, it is common to connect multiple power devices in parallel. Due to variations in the characteristics of the power devices, however, the current concentrates in part of the devices and the heat generation due to losses is localized, which degrades the reliability of the power devices. In the conventional method of parallel connection of power devices, the characteristics of the power devices are measured in advance, and power devices with matching characteristics are selected for parallel connection, which will increase the cost. Therefore, a technology to automatically equalize the current of power devices connected in parallel is required. The problem with the previous papers of current equalization is that they require a lot of ICs including such as current sensors [23–24], timing control circuits [14, 23–25], and regulators for gate voltage amplitude control [26–27], which will also increase the cost.

To solve the problems, a single-input, dual-output (SIDO) digital gate driver (DGD) IC, integrating all necessary circuits including two 6-bit

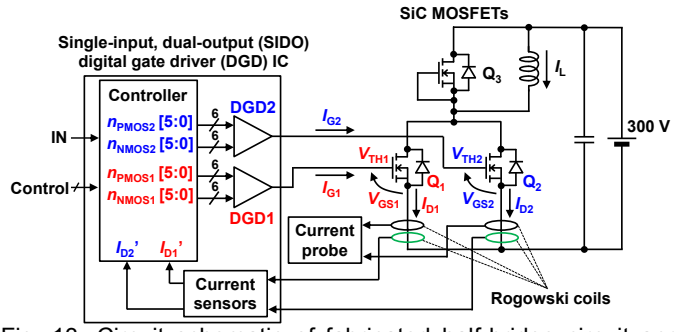


Fig. 13. Circuit schematic of fabricated half-bridge circuit and proposed SIDO DGD IC.

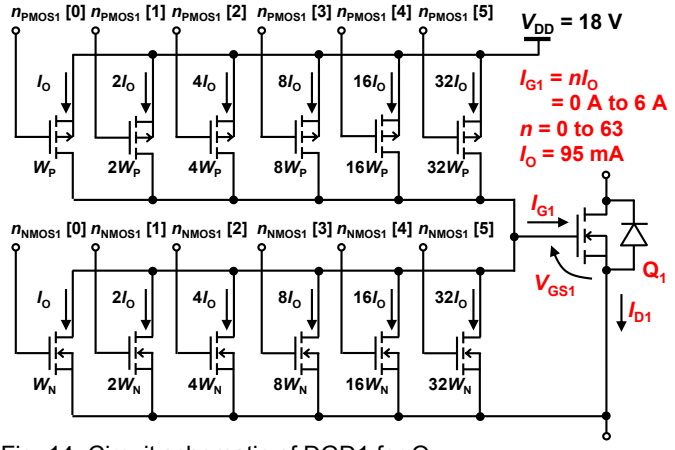


Fig. 14. Circuit schematic of DGD1 for Q_1.

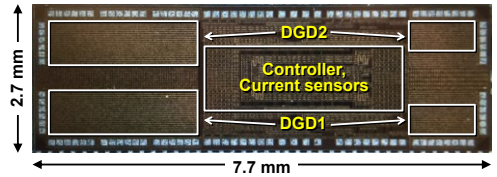


Fig. 15. Die photo of SIDO DGD IC.

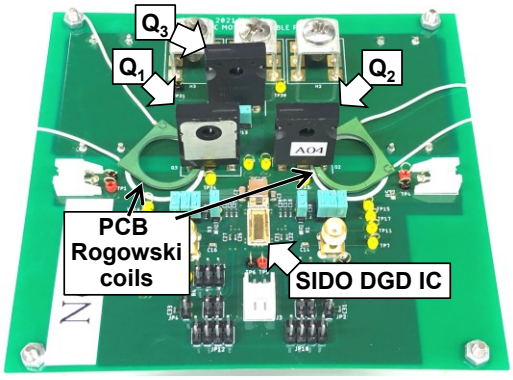


Fig. 16. Photo of PCB of half bridge.

DGDs, two current sensors, and a controller, is proposed [28] to automatically equalize the drain current (I_D) of two parallel-connected SiC MOSFETs. The proposed SIDO DGD IC will enable a high-performance power electronics systems using SiC MOSFETs at low cost, because SiC MOSFETs with large variations can be connected in parallel without prior testing and selection.

3-2 Circuit Design

Fig. 13 shows a circuit schematic of the fabricated half-bridge circuit and SIDO DGD IC. The half-bridge consists of three SiC MOSFETs (Q_1 – Q_3 : SCT3030AL, 650V, 70A) including the low-side two-parallel Q_1 and Q_2. In order to equalize DC ($I_{D1,DC}$, $I_{D2,DC}$) and surge ($I_{D1,SURGE}$, $I_{D2,SURGE}$) components of I_D of Q_1 and Q_2 (I_{D1}, I_{D2}) with

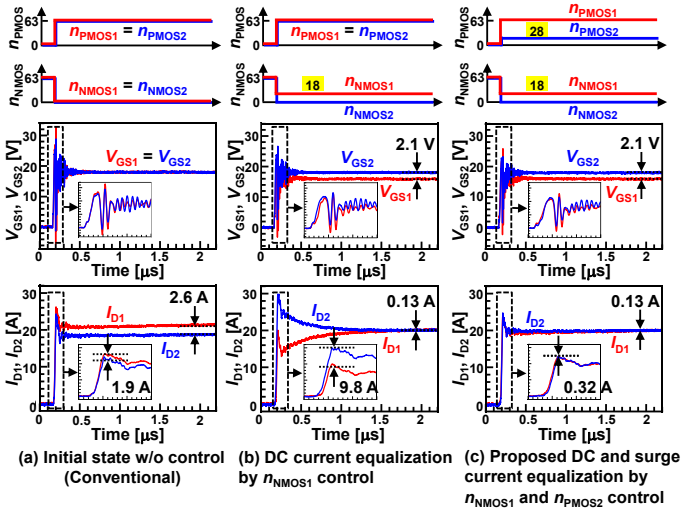


Fig. 17. Measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} at I_L = 40 A.

Table II Comparison table of DGD ICs

	TIA'17 [1]	TPEL'21 [4]	ISPSD'20 [2]	ISPSD'21 [3]	This work [28]
Target power device	Si IGBT & SiC MOSFET	GaN FET	GaN FET	GaN FET	SiC MOSFET
Process	180 nm BCD	180 nm HV CMOS	180 nm BCD	180 nm BCD	180 nm BCD
Number of outputs	1	1	1	1	2
Output voltage swing	15 V	5 V	3.3 V	5 V	18 V
Levels of I_G	6 bit	8 bit (coarse), 6 bit (fine)	7 bit	6 bit	6 bit
Max. I_G	5 A	5 V / 0.12 Ω = 42 A	3.3 V / 0.5 Ω = 6.6 A	5 A	6 A
Functions integrated into IC	1 driver	1 driver	1 driver	1 driver	2 drivers, 2 current sensors, controller
Drain current equalization of two parallel MOSFETs	No	No	No	No	Yes

variations in device characteristics by controlling the gate waveforms, SIDO DGD IC is newly developed. Except for two PCB Rogowski coils [29], all the necessary circuits including two 6-bit DGDs, two current sensors, and a controller are fully integrated into a single chip.

SIDO DGD IC has 24 bits of control bits. n_{PMOS1} [5:0] and n_{NMOS1} [5:0] control the gate current (I_{G1}) for Q_1, while n_{PMOS2} [5:0] and n_{NMOS2} [5:0] control the gate current (I_{G2}) for Q_2. Fig. 14 shows the circuit schematic of DGD1 for Q_1 in Fig. 13. I_{G1} can be varied in 64 levels at turn-on depending on 6-bit digital signals n_{PMOS1} [5:0], which is defined as n_{PMOS1}, where n_{PMOS1} is an integer between 0 and 63. The 64-level I_{G1} control from 0 A to 6 A in 95 mA increments at turn-on of Q_1 is achieved by selectively turning on or off six pMOSFETs with binary weighted gate widths (W_P, $2W_P$, $4W_P$, $8W_P$, $16W_P$, $32W_P$) in the output stage depending on n_{PMOS1} [5:0]. The same design is applied to the turn-off of Q_1 by controlling n_{NMOS1} [5:0].

3-3 Measured Results

Fig. 15 shows a die photo of SIDO DGD IC fabricated with 180-nm BCD process. Fig. 16 shows a photo of PCB of the half bridge.

Fig. 17 shows the timing chart and the measured waveforms of V_{GS1} & V_{GS2} and I_{D1} & I_{D2} at I_L = 40 A. In this work, the threshold voltage of Q_1 (V_{TH1}) is assumed to be lower than that of Q_2 (V_{TH2}). Among the eight parameters of n_{PMOS1}, n_{NMOS1}, n_{PMOS2}, and n_{NMOS2} in the on and off states of Q_1 and Q_2, n_{NMOS1} in the on state is controlled to equalize $I_{D1,DC}$ and $I_{D2,DC}$ by digitally controlling the gate voltage amplitude, and n_{PMOS2} in the on state is controlled to equalize $I_{D1,SURGE}$ and $I_{D2,SURGE}$ by digitally controlling the gate current at turn-on. Vice versa, if $V_{TH1} > V_{TH2}$, n_{NMOS2} and n_{PMOS1} are controlled. Compared with the conventional gate driving (Fig. 17 (a)), the proposed gate driving (Fig. 17 (c)) with n_{NMOS1} and n_{PMOS2} control reduces the difference

between $I_{D1,DC}$ and $I_{D2,DC}$ from 2.6 A to 0.13 A by 95% and the difference between $I_{D1,SURGE}$ and $I_{D2,SURGE}$ from 1.9 A to 0.32 A by 83%.

Table II shows a comparison table of DGD ICs. This work is the world's first IC that achieves I_D equalization of two parallel MOSFETs by integrating two DGDs, two current sensors, and a controller.

4 Large Current Output Digital Gate Driver Using Half-Bridge DAC IC and Two Power MOSFETs for IGBTs

4-1 Research Motivation

High-voltage, large-current IGBT modules (e.g. ratings of 6500 V, 1000 A) are used in many social infrastructure fields including high-voltage DC transmission systems and train traction systems [30]. In addition to improving IGBTs themselves, gate driving technologies can be used to reduce the loss of IGBTs. Recently, many papers have been published on the simultaneous reduction of both switching loss (E_{LOSS}) and switching noise by active gate waveform control using digital gate drivers (DGDs) [1-5, 31]. Conventional DGDs, however, are difficult to apply to the 6500 V, 1000 A IGBT modules, because the modules require DGD with (1) the output voltage swing (V_{SWING}) of ± 15 V to prevent a false turn-on and (2) the gate current (I_G) of up to around 20 A because of the large gate capacitance. For example, V_{SWING} is 3.3 V [2], 5 V [3–5], 15 V [1], and 18 V [31], and the maximum I_G is between 5 A [1, 3] and 42 A [4].

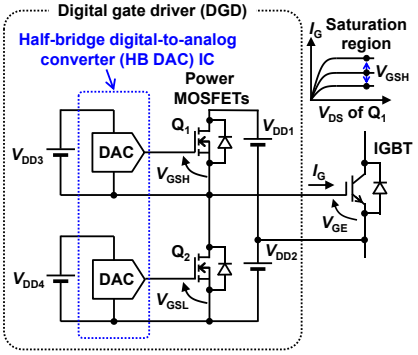


Fig. 18. Circuit schematic of proposed digital gate driver (DGD) including HB DAC IC and two power MOSFETs.

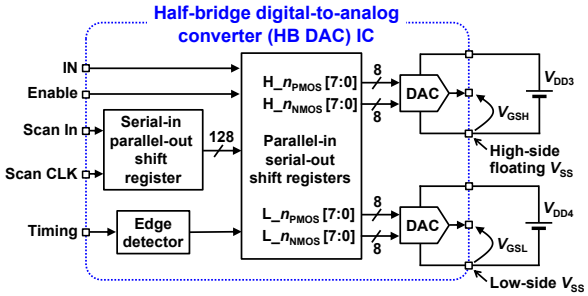


Fig. 19. Block diagram of proposed half-bridge digital-to-analog converter (HB DAC) IC.

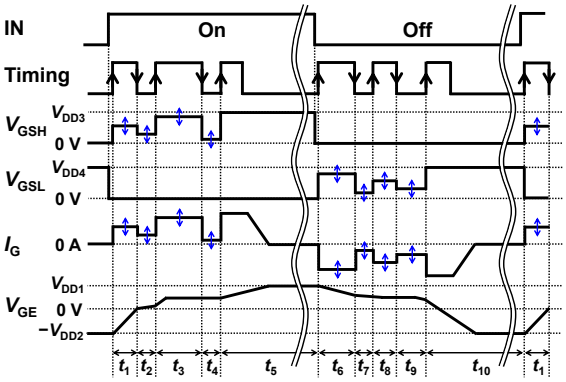


Fig. 20. Timing chart of DGD.

To solve the problems, an 8-bit DGD using a half-bridge digital-to-analog converter (HB DAC) IC and two power MOSFETs is proposed [6] to enable V_{SWING} of ± 15 V and large I_G up to 58 A for the 6500 V, 1000 A IGBT modules.

4-2 Circuit Design

Figs. 18 to 20 show a circuit schematic of the proposed DGD including HB DAC IC and two power MOSFETs (Q_1 and Q_2 : BSC094N06LS5, 60 V, 47 A), a block diagram of the proposed HB DAC IC, and a timing chart of DGD, respectively. DGD is a current-source gate driver. The novelty of this work is that power MOSFETs are used as the output stage of the gate driver to achieve large I_G, and DGD operation is achieved by digitally controlling the gate amplitude (V_{GSH} and V_{GSL}) of the power MOSFETs operating in the saturation region instead of the linear region using the proposed HB DAC IC to achieve the current-source gate driver. As shown in Fig. 19, HB DAC IC includes two DACs operating with different power supply rails, shift registers for serial inputs to reduce the number of input pins, and an edge detector to generate pulse signals from externally supplied "Timing" signal. HB DAC IC does not include the driver transistors. If all the functions are integrated into a single IC, the chip size will be huge and the cost will be high. By controlling the gate voltage of Q_1 (V_{GSH}) with a 16-bit input DAC (Fig. 19), I_G can be digitally varied four times at turn-on (Fig. 20). The four periods from t_1 to t_4 are determined by "Timing" signal, and t_1 to t_4 can be changed independently. The same is true for turn-off.

Fig. 21 shows a die micrograph of HB DAC IC fabricated with 180-nm BCD process. The die size is 2.5 mm by 1.0 mm. Fig. 22 shows a photo of PCB of DGD.

4-3 Measured Results

Fig. 23 shows a timing chart for the turn-on measurement of the conventional single-step gate driving (SGD). n is varied in SGD, where n is integers between 0 and 255. m is 60 or 100 in this work. Fig. 24 shows the measured n dependence I_G in SGD to demonstrate the successful operation of 8-bit DGD at V_{DD3} = V_{DD4} = 3.5 V and 4 V and m = 60 and 100. To investigate the performance of DGD itself, a 100 μF capacitor is connected to the output of DGD and I_G is measured. I_G is monotonically increasing with n, although it is nonlinear. The maximum I_G is 58 A.

Table III shows a comparison table of DGDs. The proposed DGD using HB DAC IC and two power MOSFETs achieves the largest

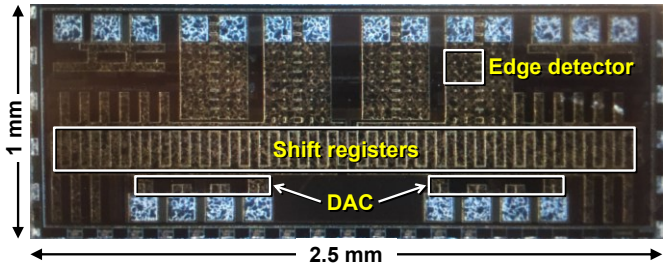


Fig. 21. Die micrograph of HB DAC IC.

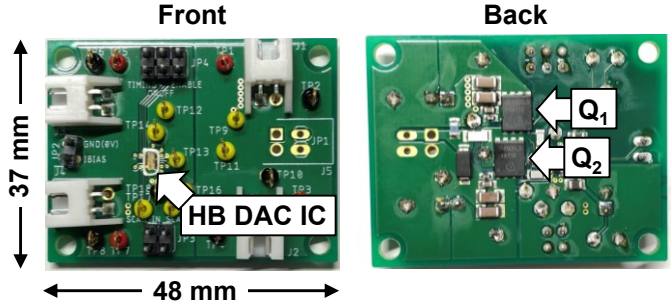


Fig. 22. Photo of PCB of DGD.

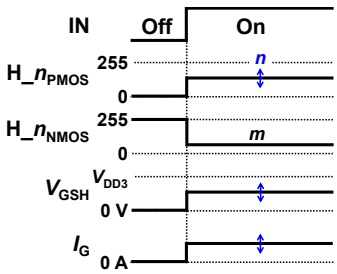


Fig. 23. Timing chart for turn-on measurement of conventional single-step gate driving (SGD).

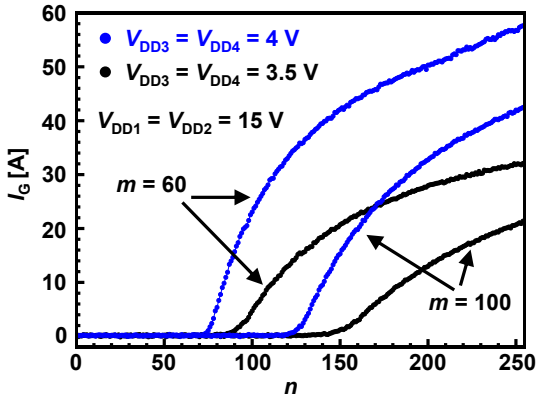


Fig. 24. Measured *n* dependence I_G in SGD to demonstrate operation of 8-bit DGD.

Table III Comparison table of DGDs

	TIA'17 [1]	ISPSD'20 [2]	ISPSD'21 [3]	TPEL'21 [4]	This work [6]
Target power device	Si IGBT & SiC MOSFET	GaN FET	GaN FET	GaN FET	Si IGBT
Process	180 nm BCD	180 nm BCD	180 nm BCD	180 nm HV CMOS	180 nm BCD
Chip area	6.25 mm²	1.97 mm²	4.32 mm²	5.0 mm²	2.5 mm²
Output voltage swing	15 V	3.3 V	5 V	5 V	30 V
Levels of I_G	6 bit	7 bit	6 bit	8 bit (coarse), 6 bit (fine)	8 bit
Max. I_G	5 A	3.3 V / 0.5 Ω = 6.6 A	5 A	5 V / 0.12 Ω = 42 A	58 A
Functions integrated into IC	1 driver	1 driver	1 driver	1 driver	2 DACs

V_{SWING} of 30 V and the largest I_G of 58 A in DGDs. This work is the first to demonstrate the advantages of DGD in the high-voltage, large-current IGBT modules.

5 Summary and Future Design Challenges

This paper presents the digital gate driver IC with automatic timing control, the single-input dual-output digital gate driver IC for equalizing drain current of two parallel-connected SiC MOSFETs, and the large current output digital gate driver, which were developed to achieve a networked digital gate IC by driving and sensing power devices.

Future design challenges for the digital gate ICs include: (1) sensing technology for the operating and degradation states of power devices via gate terminals to achieve integrated sensor circuits; (2) integration of signal isolators and isolated power supplies into ICs to eliminate external bulky transformers; and (3) development of algorithms to determine digital gate driver parameters based on sensor output to meet customer needs such as loss reduction, noise reduction, and failure prediction.

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